Introduction

Intersil Real Time Clock (RTC) products now include a low cost set of products that strike a balance of features and performance for a wide variety of applications. Formerly the devices in the RTC product line used EEPROM cells for registers and general purpose memory. The new devices use battery-backed SRAM for all memory which results in a lower cost, yet very reliable, RTC device.

The family of devices is summarized in Table 1, indicating the features available in each device. New features include the InterSeal battery preservation function, event detection and time stamp (on some products) and an oscillator on/off control. We will cover these features as well as some general applications guidelines for the devices.

Summary of Device Functions

InterSeal Operation

This function is simply the ability of the device to draw zero current from the battery until the device has had V_{DD} power applied as well as V_{BAT}. Most product applications will have a battery installed during assembly, and this will bias the VBAT pin until the V_{DD} is applied when assembly is completed. In some cases the battery can be installed in the device after assembly and electrical testing is completed. This will allow zero current drain until the product is actually put into use for the first time and also will allow maximum shelf life for products that may spend a period of time idle after manufacturing and initial operation.

Time Clock Function

The RTC function includes a clock/calendar and one alarm, which uses a set of registers for control, status and programming. These registers provide seconds, minutes, hours, day of the week, month, and year, with automatic correction for leap years. The clock format is selectable for either AM/PM or 24-hour (military) format. On initial power-up, the clock will not function until at least one byte is written to the clock/calendar registers.

Alarm Operation

The Alarm function generates an alarm once every minute, hour, day, week, month or year. There is one alarm register set that has essentially the same format as the clock/calendar registers. Once the alarm register matches the clock/calendar setting, an alarm flag is set in the main status register for software interrupts. The alarm can also initiate a hardware interrupt via the $\overline{IRQ}$ pin. In order for that to occur, devices with a shared $\overline{IRQ}/F_{OUT}$ pin need to have the frequency output disabled. Those devices with separate $\overline{IRQ}$ and F_{OUT} pins will always have a hardware interrupt pin available.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

1. **Single Event Mode** is enabled by setting the ALME bit to "1", the IM bit to "0", and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to "1" and the $\overline{IRQ}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
2. **Interrupt Mode** (also called PIM) is enabled by setting the ALME bit to "1", the IM bit to "1", and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time.

An example of interrupt mode is setting just the seconds register to "00h" and enabling the alarm and $\overline{IRQ}$ output. Then the $\overline{IRQ}$ will trigger once per minute. Interrupt mode is also convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading. Note that interrupt mode is NOT a timer function so exact time-out periods cannot be programmed, only RTC register matches.

However, the PIM Mode can be used for exact oscillator accuracy measurement. For example, if the seconds register only is set for alarm and PIM is enabled, then the $\overline{IRQ}$ output will be exactly 1 minute, and if a frequency counter is used to measure the pulses, the result will reflect the accuracy of the oscillator.

To clear an alarm, the ALM bit in the status register must be set to "0" with a write. Note that if the ARST bit is set to "1" (address 07h, bit 7), the ALM bit will automatically be cleared when the status register is read.

TABLE 1. INTERSIL RTC PRODUCT FAMILY

PRODUCT	INTERSEAL?	# ALARMS	EVENT DETECTION	EVENT TIME STAMP	CLOCK FREQUENCY OUTPUT	SEPARATE F_{OUT} PIN	ON-CHIP OSCILLATOR COMPENSATION	GENERAL PURPOSE SRAM	PACKAGES
ISL1208	Yes	1	No	No	Yes	No	Yes	2x8 bits	8 Ld MSOP, SO
ISL1209	Yes	1	Yes	No	Yes	No	Yes	2x8 bits	10 Ld MSOP
ISL1218	Yes	1	No	No	Yes	No	Yes	8x8 bits	8 Ld MSOP, SO
ISL1219	Yes	1	Yes*	Yes	Yes	No	Yes	2x8 bits	10 Ld MSOP
ISL1220	Yes	1	No	No	Yes	Yes	Yes	8x8 bits	10 Ld MSOP
ISL1221	Yes	1	Yes*	Yes	Yes	Yes	Yes	2x8 bits	10 Ld MSOP

Frequency Output

This is the F_{OUT} pin noted on the data sheets and shares pin functionality with the $\overline{IRQ}$ function on some devices. When the F_{OUT} function is enabled, the $\overline{IRQ}$ function is disabled. Four bits in the control registers (FO0 to FO3) select the functionality for this pin, as shown in Table 2.

TABLE 2. F_{OUT} OUTPUT CONTROL

FREQUENCY, F_{OUT}	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

The F_{OUT} function can be used for clocking other devices in the system, or as an accurate counter for miscellaneous timing functions. It is also very useful for calibrating the oscillator frequency as described in the “Crystal Oscillator Frequency Adjustment” on page 5.

The Frequency output pin is an open drain and requires a pull-up resistor. For low frequency signals of <1024Hz, 50kΩ or greater values can be used. For accurate 32kHz clocking, a 2.2kΩ pull-up is advised. The FOBATB bit in the INT register controls whether the F_{OUT} pin is active in battery backup. When the FOBATB is set to “1”, the F_{OUT} pin is disabled during battery backup mode. When the FOBATB is cleared to “0”, the F_{OUT} pin is enabled during battery backup mode. Thus, when used in battery backup mode, F_{OUT} requires a pull-up resistor to V_{BAT}.

When adding the RTC device to a PC board layout, care should be taken to route the F_{OUT} trace away from the crystal (preferably have a ground or power trace between the crystal and F_{OUT}). This will minimize the noise pickup at the X1/X2 pins, which contributes to clock accuracy errors.

Serial Data Interface

The serial interface consists of clock and data (SCL and SDA pins) and meets the timing and pin voltage requirements of the I^2C interface. Start and stop conditions are used along with acknowledge on address and data transfers. The devices can be used with clock frequencies up to 400kHz. The SDA output is open drain and the serial bus line needs a pull-up resistor somewhere on the board for proper operation. It is highly recommended that the serial interface pull-up resistors are tied to V_{DD} and that V_{DD} needs to go to 0V or very close to 0V when powered down to avoid excessive battery current drain.

The serial interface will operate down to the point of battery switchover. The serial interface does not operate in battery backup mode. Note that there is a control bit, LPMODE, that when set to “1” allows battery switchover at $V_{DD} < V_{BAT}$. In the case where V_{BAT} = 0V (grounded input), then the serial interface will work down to the guaranteed operating point of 1.8V, with the restriction that the V_{IH} and V_{IL} logic level limits are not guaranteed so tighter parameters should be considered. Otherwise, the normal minimum power supply for serial interface is V_{DD} = 2.7V.

When adding the RTC device to a PC board layout, care should be taken to route the SCL and SDA traces away from the crystal, preferably have a ground or power trace between the crystal and F_{OUT}. This will minimize the noise pickup at the X1/X2 pins which contributes to clock accuracy errors.

Battery Backup Switchover Circuit

There are two power supply pins for each RTC device, V_{DD} and V_{BAT}. The V_{DD} pin is for the main board power supply of from 2.7V to 5.5V. The V_{BAT} pin is for a backup supply dedicated for the RTC chip. The pin can be tied to a battery, a supercap, or tied to ground if not used. The RTC devices contain internal circuitry to automatically switchover to the backup battery when the main V_{DD} supply fails, and switch back from battery to V_{DD} when the main supply recovers (see Figure 1). This circuit contains hysteresis to address noise and glitch issues in V_{DD} lines. There is approximately 50mV of hysteresis in the voltage comparator when switching from V_{DD} to V_{BAT}, and 50mV of when switching from V_{BAT} to V_{DD}.

If the V_{BAT} input is not used, it should be tied to ground, not to V_{DD}.

LOW POWER MODE

The RTC devices are designed to switch into battery backup mode only if the V_{DD} power is lost (dropping below V_{TRIP} and close to 0.0V). Another mode, called Low Power Mode, is available to allow direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below V_{TRIP}. Since the additional monitoring of V_{DD} vs V_{TRIP} is no longer needed, that circuitry is shut down and less power is used while operating from V_{DD}. Power savings are typically 600nA at V_{DD} = 5V. Low Power Mode is activated by setting the LPMODE bit in the control and status registers to “1”.

Low Power Mode is useful in systems where V_{DD} is normally higher than V_{BAT} at all times. The device will switch from V_{DD} to V_{BAT} when V_{DD} drops below V_{BAT}, with about 50mV of hysteresis to prevent any switchback of V_{DD} after switchover. In a system with a V_{DD} = 5V and backup lithium battery of V_{BAT} = 3V, Low Power Mode can be used. However, **DO NOT USE** Low Power Mode in a system with V_{DD} = 3.3V ±10%, $V_{BAT} \geq$ 3.0V, and when there is a finite I-R voltage drop in the V_{DD} line, or intermittent serial bus operation may result.

UL LISTING

Since Lithium batteries are often used for battery backup, knowledge of the backup circuitry is required for Underwriters Laboratories approval. Figure 1 shows the internal switchover circuitry illustrating the complementary control which disables one input while enabling the other. There are redundant transistors in the path from V_{DD} to V_{BAT}, plus a small series resistor in the V_{BAT} circuit. Leakage from V_{DD} to V_{BAT} normally is negligible (<100nA) and if a single point failure were to occur, the resulting Lithium charging current is within UL specifications. The ISL1208 series of RTC devices are UL recognized for Lithium battery connections with restrictions on maximum charging current (16mA at V_{DD} = 5.5V and 13mA at V_{DD} = 3.6V). If a series Schottky diode is added to the V_{BAT} input then the circuit will meet full UL requirements.

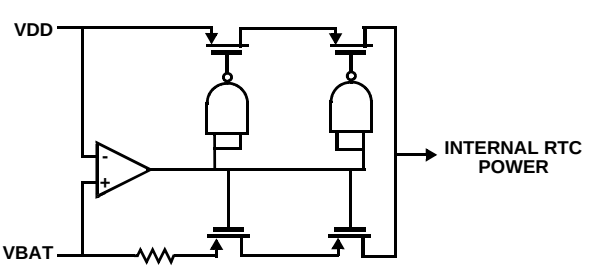

FIGURE 1. SIMPLIFIED BATTERY SWITCHOVER CIRCUIT

V_{DD} RAMP RATES AND GLITCH DETECTION

The data sheet specifies a -10V/ms maximum negative slew rate (power down V_{DD} ramp rate). This should be followed to avoid losing any of the RAM register settings during power-down. If the negative slew rate is excessive, then the internal power node voltages can droop during switchover, causing the SRAM cells to change state or erase. In most systems this is not an issue but the V_{DD} power-down waveform should be observed as a precaution.

If the V_{DD} power-down timing is exceedingly fast, a simple fix is to add an RC network to the V_{DD} pin. Since the supply current for the device is very low, series resistance of up to 1kΩ can be added, and choice of a capacitor value is left to the designer. Typically, 0.47µF can be used but lower values are possible depending on the existing V_{DD} slew rate.

The V_{DD}/V_{BAT} power circuit also contains a glitch detection circuit to protect from incorrect serial bus writes after a brownout situation. This circuit disables the serial bus for about 90ms following the power-up. To trigger the delay, the V_{DD} must drop below the battery trip point yet stay above approximately 1.0V (limit of active circuit operation). After that, the power-up ramp must be slower than 0.25V/ms to trigger the delay. To be safe, serial interface software may need to consider the 90ms delay in all power-up routines. (**Note**: Early production quantities of the ISL1208 and ISL1209 had a longer delay of 3.0s, which was changed to 90ms for current production).

Some battery backup circuits may have high series resistance, added in some cases to isolate the battery circuit from the RTC. There are limits to the amount of series resistance that can work with the RTC, since there may be a small surge of current during battery switchover which may cause the backup battery supply voltage to droop dangerously low.

Backup Battery Operation

Many types of backup supplies can be used with the ISL1208 series RTC devices.

LITHIUM COIN CELLS

3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power a Intersil RTC device for up to 10 years. The battery can simply be connected to the V_{BAT} input and ground for backup battery power. It is possible to

use a 3.6V battery with V_{DD} = 3.3V, with the only restriction being that the LPMODE bit = “0” (normal mode) to prevent hanging up the serial interface. Note that if a lithium coin cell is inserted into a holder after a board has been tested and powered down, then the InterSeal function will prevent any battery drain until the unit is first powered up in actual use.

SUPERCAPACITORS

The RTC devices provide a V_{BAT} pin which is used for a battery backup input. A supercapacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the RTC is extremely low, it is possible to get months of backup operation using a supercapacitor. Typical capacitor values are a few µF to 1F or more depending on the application.

If backup is only needed for a few minutes, then a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity supercapacitor is the best choice. These devices are available from such vendors as Panasonic and Murata. The main specifications include working voltage and leakage current. If the application is for charging the capacitor from a +5V ±5% supply with a signal diode, then the voltage on the capacitor can vary from ~4.5V to slightly over 5.0V. A capacitor with a rated WV of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible. For example, a supercapacitor should be specified with leakage of well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

Following are some examples with equations to assist with calculating backup times and required capacitance for the ISL1219 device. The backup supply current plays a major part in these equations, and a typical value was chosen for example purposes. For a robust design, a margin of 30% should be included to cover supply current and capacitance tolerances over the results of the calculations. Even more margin should be included if periods of very warm temperature operation are expected.

Example 1. Calculating Backup Time Given Voltages and Capacitor Value

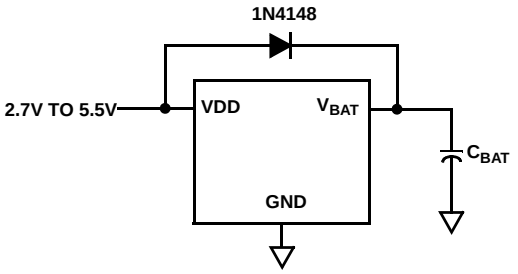

FIGURE 2. SUPERCAPACITOR CHARGING CIRCUIT

In Figure 2, use C_{BAT} = 0.47F and V_{DD} = 5.0V. With V_{DD} = 5.0V, the voltage at V_{BAT} will approach 4.7V as the diode turns off completely. The ISL1219 is specified to operate down to V_{BAT} = 1.8V. The capacitance charge/discharge (see Equation 1) is used to estimate the total backup time:

$$I = C_{BAT} * dV/dT \quad \text{(EQ. 1)}$$

Rearranging gives Equation 2:

$$dT = C_{BAT} * dV/I_{TOT} \text{ to solve for backup time.} \quad \text{(EQ. 2)}$$

C_{BAT} is the backup capacitance and dV is the change in voltage from fully charged to loss of operation. Note that I_{TOT} is the total of the supply current of the ISL1219 (I_{BAT}) plus the leakage current of the capacitor and the diode, I_{LKG}. In these calculations, I_{LKG} is assumed to be extremely small and will be ignored. If an application requires extended operation at temperatures over +50°C, these leakages will increase and hence reduce backup time.

Note that I_{BAT} changes with V_{BAT} almost linearly (Refer to the Typical Performance Curves in the datasheet). This allows us to make an approximation of I_{BAT}, using a value midway between the two endpoints. The typical linear equation for I_{BAT} vs V_{BAT} is shown in Equation 3:

$$I_{BAT} = 1.031E\text{-}7*(V_{BAT}) + 1.036E\text{-}7A \quad \text{(EQ. 3)}$$

Using Equation 4 to solve for the average current given 2 voltage points calculates:

$$I_{BATAVG} = 5.155E\text{-}8*(V_{BAT2} + V_{BAT1}) + 1.036E\text{-}7A \quad \text{(EQ. 4)}$$

Combining with Equation 2 gives the equation for backup time:

$$T_{BACKUP} = C_{BAT}*(V_{BAT2} - V_{BAT1})/(I_{BATAVG} + I_{LKG}) \text{ seconds} \quad \text{(EQ. 5)}$$

where:

C_{BAT} = 0.47F

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

I_{LKG} = 0 (assumed minimal)

Solving Equation 4 for this example, I_{BATAVG} = 4.387E-7A in Equation 6:

$$T_{BACKUP} = 0.47 * (2.9)/4.38E\text{-}7A = 3.107E6s \quad \text{(EQ. 6)}$$

Since there are 86,400 seconds in a day, this corresponds to 35.96 days. If the 30% tolerance is included for capacitor and supply current tolerances, then worst case backup time would be shown in Equation 7:

$$C_{BAT} = 0.70*35.96 = 25.2 \text{ days} \quad \text{(EQ. 7)}$$

Example 2. Calculating a Capacitor Value for a Given Backup Time

Referring to Figure 2 again, the capacitor value needs to be calculated to give 2 months (60 days) of backup time, given V_{DD} = 5.0V. As in Example 1, the V_{BAT} voltage will vary from 4.7V down to 1.8V. We will need to rearrange Equation 2 to solve for capacitance shown in Equation 8:

$$C_{BAT} = dT*I/dV \quad \text{(EQ. 8)}$$

Using the terms described in Equation 8, this becomes Equation 9:

$$C_{BAT} = T_{BACKUP}*(I_{BATAVG} + I_{LKG})/(V_{BAT2} - V_{BAT1}) \quad \text{(EQ. 9)}$$

where:

T_{BACKUP} = 60 days*86,400 sec/day = 5.18 E6s

I_{BATAVG} = 4.387 E-7A (same as Example 1)

I_{LKG} = 0 (assumed)

V_{BAT2} = 4.7V

V_{BAT1} = 1.8V

Solving gives Equation 10:

$$C_{BAT} = 5.18\ E6*(4.387\ E-7)/(2.9) = 0.784F \quad \text{(EQ. 10)}$$

If the 30% tolerance is included for tolerances, then worst case capacitor value would be Equation 11:

$$C_{BAT} = 1.3*0.784 = 1.02F \quad \text{(EQ. 11)}$$

Care must be taken if a supercapacitor is used in Low Power Mode. Although there is a series diode in the supercapacitor charging circuit which drops the voltage to below V_{DD}, in some instances V_{DD} changes can occur which may exceed the 50mV switchover hysteresis. If that occurs and the device is in Low Power Mode, then the device will enter backup mode and the serial interface will stop operating momentarily until the V_{DD} power recovers or the supercapacitor discharges.

Using an External Clock

To use an external clock with the ISL1208 family follow these requirements:

1. Apply the proper input to the X1 pin. The clock must be logic level CMOS (0.3 x V_{DD} max V_{IN} LOW, 0.7 x V_{DD} V_{IN} HIGH), square wave preferred, Frequency = 32768.0Hz

2. Set the XTOSCB (external oscillator control) bit in Register 07h to “1”. This disables the crystal oscillator and enables the X1 input as a clock input. Since register 07h is the Status Register, make sure that the other bits are set properly.

3. Make sure the external clock is working properly. You may either poll the time registers to make sure the seconds are advancing at the correct rate, or turn on the frequency output and monitor the frequency for the correct value.

The clock signal used for the X1 input should come from a source with the same V_{DD} as the ISL1208 series device. Otherwise, applying a voltage to the X1 pin with no power applied to V_{DD} may damage the device.

Oscillator Crystal Requirements

The RTC devices use a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. The only hard restriction on specifications for the crystal is the load capacitance, which must be 12.5pF. Any other value will cause excessive accuracy errors. The ESR should be <50kΩ, although higher values operate fine (start-up time will increase at high ESR).

Table 3 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the RTC device if their specifications are very similar to the devices listed. The crystal’s temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

TABLE 3. SUGGESTED SURFACE MOUNT CRYSTALS

MANUFACTURER	PART NUMBER
Citizen	CM200S
Epson	MC-306, MC-406
Raltron	RSM-200S
ECS	ECX-306X
Fox	FSM-327

Crystal Oscillator Frequency Adjustment

The RTC devices contains circuitry for adjusting the frequency of the crystal oscillator. This circuitry can be used to trim oscillator initial accuracy as well as adjust the frequency to compensate for temperature changes.

The Analog Trimming Register (ATR) is used to adjust the load capacitance seen by the crystal. There are six bits of ATR control, with linear capacitance increments available for adjustment. Since the ATR adjustment is essentially “pulling” the frequency of the oscillator, the resulting frequency changes will not be linear with incremental capacitance changes. The equations which govern pulling show that lower capacitor values of ATR adjustment will provide larger increments. Also, the higher values of ATR adjustment will produce smaller incremental frequency changes. These values typically vary from 6ppm to 10ppm/bit at the low end to <1ppm/bit at the highest capacitance settings. A typical curve showing the ATR control characteristic is shown in Figure 3.

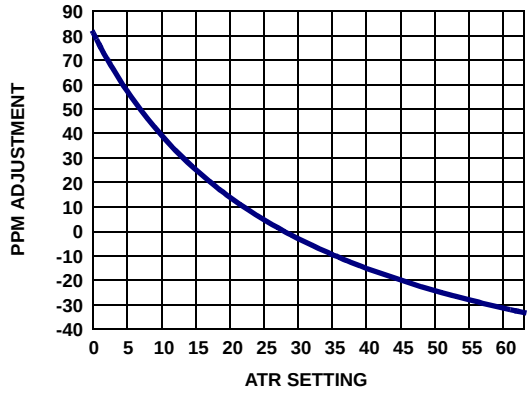

FIGURE 3. ATR SETTING vs OSCILLATOR FREQUENCY ADJUSTMENT

The range afforded by the ATR adjustment with a typical surface mount crystal is typically -33ppm to +80ppm relative to ATR = 0 (measured at room temperature). This will vary from device to device and depends also on the PC board layout (the user should note this when using the ATR for calibration). The temperature drift of the capacitance used in the ATR control is extremely low, so this feature can be used for temperature compensation with good accuracy.

DTR (Digital Trimming Register) F_{OUT} effects

In addition to the analog compensation afforded by the adjustable load capacitance, a digital frequency compensation feature is available for the ISL1219. The Digital Trimming Register (DTR) controls digital compensation. The range provided is ±60ppm in increments of 20ppm. DTR adds or skips pulses in the clock counter. It is very useful for coarse adjustments of frequency drift over-temperature or extending the adjustment range available with the ATR register.

Since the overall frequency change using DTR is so small and there are only so many pulses/second, dithering is done at 20/40ppm setting for DTR. If the engineer is trying to set and measure short term change in frequency using the F_{OUT} pin, the results are not straightforward. Here is what will be measured at F_{OUT}:

- ±20ppm: gives either ±30ppm or ±15ppm
- ±40ppm: gives either ±45ppm or ±30ppm
- ±60ppm: gives ONLY ±60ppm (no dithering)

Note that the overall adjustment is very exact, so if F_{OUT} is measured in production, the ATR adjustment can be measured quickly with a frequency counter, and the DTR setting can just be added/subtracted on top of that.

Measuring Oscillator Frequency Accuracy

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the $\overline{IRQ}/F_{OUT}$ pin with a calibrated frequency counter. (Note: DO NOT use a scope probe on the X2 pin to monitor the oscillator waveform for this purpose. Even with a low capacitance probe there will be accuracy error induced!)

The frequency used is unimportant, although 1Hz is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The ATR should be set to the center position, or 100000b, to begin with. Once the initial measurement is made, then the ATR register can be changed to adjust the frequency. Note that increasing the ATR register for increased capacitance will lower the frequency, and vice-versa. If the initial measurement shows the frequency is far off, it may be necessary to use the DTR register to do a coarse adjustment. Note that most all crystals will have tight enough initial accuracy at room temperature so that a small ATR register adjustment should be all that is needed.

Intersil has developed a hardware calibration setup using Labview to set the initial accuracy of an RTC device on a production board. Please contact factory applications for details.

Temperature Compensation

The ATR and DTR controls can be combined to provide crystal drift temperature compensation. The typical 32.768kHz crystal has a drift characteristic that is similar to that shown in Figure 4. There is a turnover temperature (T_0) at the apex where the drift is very near zero. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature.

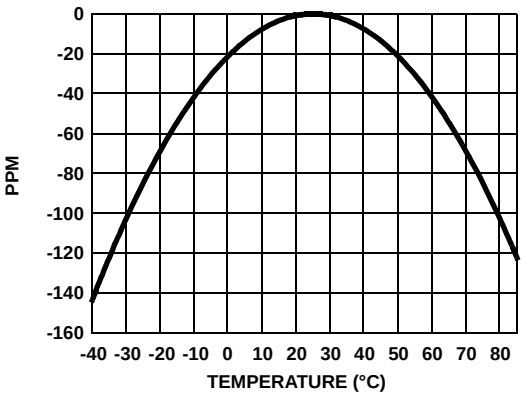

FIGURE 4. RTC CRYSTAL TEMPERATURE DRIFT

If full industrial temperature compensation is desired in an RTC circuit, then both the DTR and ATR registers will need to be utilized (total correction range typical = -93ppm to +140ppm).

A system to implement temperature compensation would consist of the ISL1219, a temperature sensor, and a microcontroller. These devices may already be in the system so the function will just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal manufacturer's specifications for the turnover temperature T_0 and the drift coefficient (β). The formula for

calculating the oscillator adjustment necessary is shown in Equation 12:

$$\text{Adjustment (ppm)} = -(T - T_0)^2 * \beta \quad \text{(EQ. 12)}$$

Once the temperature curve for a crystal is established, then the designer should decide at what discrete temperatures the compensation will change. Since drift is higher at extreme temperatures, the compensation may not be needed until the temperature is greater than +20°C from T_0. The ATR adjustment curve in Figure 3 should be used, along with DTR adjustment, to set frequency correction over-temperature. The values indicated would be placed in a lookup table for the microcontroller to access.

Layout Considerations

The crystal input at X1 has a very high impedance, with a low level analog sine wave of 300mV to 400mV. Oscillator circuits operating at low frequencies such as 32.768kHz are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines, including the PC traces for SCL and SDA. Careful layout of the RTC circuit will avoid noise pickup and insure accurate clocking.

Figure 5 shows a suggested layout for the ISL1208 or ISL1218 devices using a surface mount crystal. The other devices can use a similar layout. Two main precautions should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

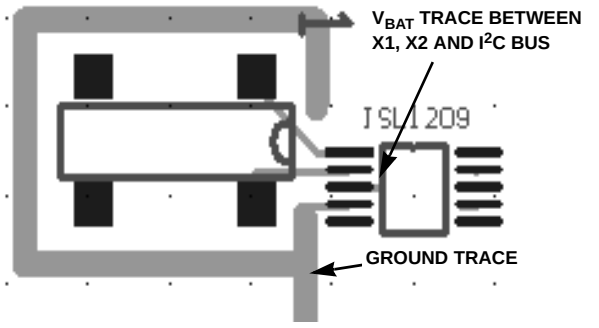

FIGURE 5. SUGGESTED LAYOUT FOR ISL1219 AND CRYSTAL

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ}/F_{OUT}$ pin (or F_{OUT} pin for ISL1220, ISL1221) is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{DD} pins can be treated as a ground, and can be routed around the crystal.

It is always a good idea to add a decoupling capacitor close to the V_{DD} pin, especially if a low value pull-up resistor is on the F_{OUT} pin.

Event Detection

The ISL1209, ISL1219 and ISL1221 have an event detection feature intended to be used for recording the time of single events that involve the opening of an enclosure, door, etc. The normal method of detection is with normally closed switch function that opens to initiate the event. This mechanism is ideal for applications such as set top boxes, utility meters, security alarm and camera systems or vending machines.

Note that the ISL1219 and ISL1221 devices contain a set of timestamp registers to record the initial, single event. The ISL1209 device does not have the timestamp registers, and will only record a bit indicating an event happened. It also has the option of stopping the RTC clock upon event detection, which will record the event time but real time clocking will cease.

A “Typical Application Diagram” on page 8 is shown in Figure 6. A microcontroller communicates with the ISL1219 through the I^2C serial bus, to set-up and read time of the day, alarms, or set-up the outputs frequency control.

The ISL1219, ISL1221 are capable of recording individual event time/dates using the on-chip registers (Event Registers, addresses 14h to 19h). Single event times are recorded and can be read using a multiple address read, similar to reading the RTC registers. The Event Registers record the initial event time of a series of events, until the EVT bit is reset. After EVT is reset, the Timestamp Registers retain the previous event time until the next Event happens, at which time the current RTC register contents will be placed in the Event Registers. The Timestamp Registers cannot be cleared, only a full power-down cycle (V_{CC} and V_{BAT} = 0V) will erase their contents.

For example, the event function is enabled and the EVT bit in the Status Register is cleared. Then the EVEN pin is triggered 3x before the timestamp register is read. Only the first Event time will be recorded in the Timestamp Registers, and will be read. Then the EVT bit is cleared in the Status Register, and two more events happen. The previous Timestamp contents are replaced by the time of the next event after the EVT bit reset.

The ISL1209, ISL1219, ISL1221 all can be set to stop the real time clock from advancing. If the event register is set to enable this function (Register 09h, RTCHLT bit 5 set to 1), then when the EVIN pin is triggered, the clock counters will stop and hold the time of the event. This is useful for one

time occurrences such as opening a warranted consumer product enclosure or exceeding a maximum temperature inside a device. Once the clock is stopped, the clock registers must be written with an updated time, then they will begin advancing immediately. If the RTCHLT bit is still set, then the next event will again stop the clock.

EVENT DETECT INPUT DETAILS

The EVIN input is a Schmitt trigger logic input. An event is detected when it is asserted high. The RTC device has internal configuration settings, which add detection flexibility. There are four configuration bits in register 09h which are for EVIN sampling. The ESMP1 and ESMP0 bits control sampling of the event input status. Reducing the sampling rate will lower the supply current drain, with the trade-off of adding a delay in detecting an event. An event that is long in duration (i.e. opening a door) would obviously be served well with the lowest frequency sampling rate and lowest supply current drain.

The EHYS1 and EHYS0 bits control timer circuits to filter out switch bouncing, noise or intermittent contacts, by effectively adding time-based hysteresis to the EVIN input. They are used only in conjunction with the sampling rate; they cannot be used alone.

EVENT BATTERY BACKUP DETAILS

The event detection function has been designed to minimize power drain for extended life in battery backed applications. Many applications will need detection while in battery backup. The EVBATB bit is used to enable the event input in battery backup mode. Note that to DISABLE event sampling in battery backup, this bit is set to “1”. After power is shut off, the occurrence of an event is recorded and can be read by the microprocessor the next time the circuit is powered up. The input current sources and sampling are also usable in battery backup mode. If the EVIENB bit is set to disable the input current source, a large value pull-up resistor (to minimize battery drain) must be tied to the V_{BAT} input to allow event detection in battery backup.

Note that any input signal conditioning circuitry that is added in regular operation or battery backup should have minimum supply current drain, or have the capability to be put in a low power standby mode. The ISL28914 is a rail-to-rail op amp with exceptionally low supply current (330nA) and so it is ideal for use in battery backup applications.

Summary

The Intersil RTC product family integrates the clock/calendar function, alarms, battery backup circuit and precision crystal compensation into a single device. The device also draws very low battery current insuring long life in remote applications. This functional integration is crucial to applications where clock accuracy and long field life are needed, such as medical systems, utility meters, security surveillance systems and network equipment. The small packages offered along with the low parts count also make the devices ideal for handheld applications.

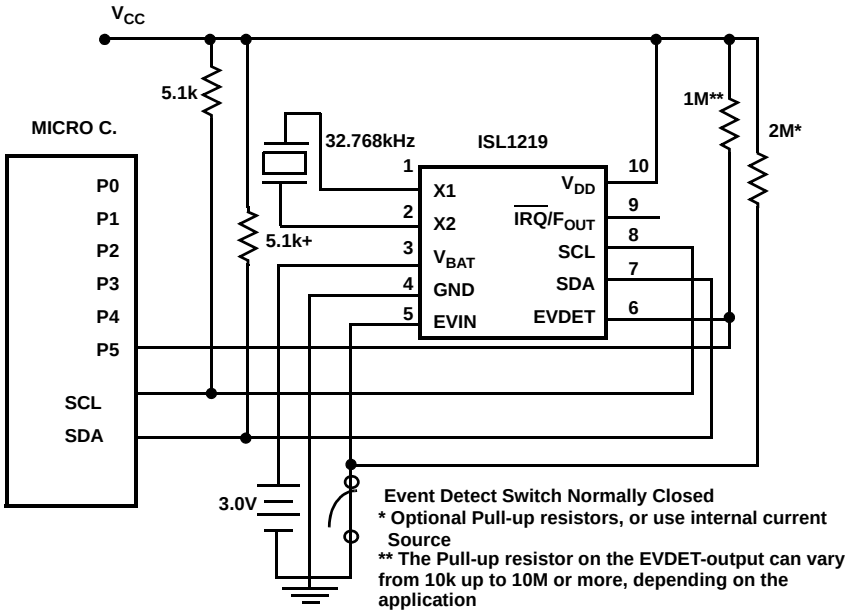

FIGURE 6. TYPICAL APPLICATION DIAGRAM